We claim:

1. A cache memory, comprising:

a plurality of cache lines for storing a value from main memory; and

a timer associated with each of said plurality of cache lines, each of said timers configured to control a signal that removes power to said associated cache line after a decay interval.

2. The cache memory of claim 1, wherein a timer associated with a given cache line is reset each time said associated cache line is accessed.

3. The cache memory of claim 1, wherein said decay interval is variable.

4. The cache memory of claim 3, wherein said variable decay interval can be increased to increase performance.

5. The cache memory of claim 3, wherein said variable decay interval can be lowered to save power.

6. The cache memory of claim 3, wherein said variable decay interval is implemented by adjusting a reference value in a comparator.

7. The cache memory of claim 3, wherein said variable decay interval is implemented by adjusting a bias of a comparator.

8. The cache memory of claim 1, wherein said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N.

9. The cache memory of claim 1, wherein said timer is a k bit timer and said timer receives a tick from any source.

10. The cache memory of claim 1, wherein said timer is any k-state finite state machine (FSM) that can function logically as a counter.

11. The cache memory of claim 1, further comprising a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval.

12. The cache memory of claim 11, wherein one or more of said timers associated with said plurality of cache lines are cascaded to distribute said writing back to main memory over time.

13. The cache memory of claim 1, wherein said removing power from said associated cache line resets a valid field associated with said cache line.

14. The cache memory of claim 1, wherein said signal is further configured to remove a potential from said cache line.

15. The cache memory of claim 1, wherein a first access to a cache line that has been powered down results in a cache miss, resets said corresponding timer and restores power to said cache line.

16. The cache memory of claim 1, wherein a first access to a cache line that has been powered down is delayed by a period of time that permits said cache line to stabilize after power is restored.

17. The cache memory of claim 1, wherein said timer is an analog device that detects a predefined voltage on said device corresponding to said decay interval.

18. The cache memory of claim 1, wherein said cache memory is a multilevel cache memory, and further comprising one or more inclusion bits associated with each of said cache lines, said inclusion bits indicating whether data stored in said cache line exists in upper levels and wherein said power is removed only from a data field associated with said cache line after said decay interval when said inclusion bits indicate the existence of the same data in an upper level.

19. The cache memory of claim 1, wherein said cache memory is a multilevel cache memory, and wherein said power is removed from a cache line after said decay interval only if said power is removed in corresponding upper levels of said multilevel cache memory.

20. A method for reducing leakage power in a cache memory, said cache memory having a plurality of cache lines, said method comprising the steps of:

providing a timer for each of said cache lines;

resetting said timer each time said cache line is accessed; and

removing power from said associated cache line after a decay interval.

21. The method of claim 20, wherein said decay interval is variable.

22. The method of claim 20, wherein said timer is a k-bit timer and said timer receives a tick from a global N-bit counter where k is less than N.

23. The method of claim 20, further comprising the step of evaluating a dirty bit associated with each of said cache lines that indicates when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval.

24. The method of claim 20, wherein said step of removing power from said associated cache line further comprises the step of resetting a valid field associated with said cache line.

25. The method of claim 20, wherein a first access to a cache line that has been powered down further comprises the steps of establishing a cache miss, resetting said corresponding timer and restoring power to said cache line.

26. The method of claim 20, wherein a first access to a cache line that has been powered down further comprises the step of delaying said access by an appropriate amount of time until said cache line stabilizes after power is restored.

27. A cache memory, comprising:

a plurality of cache lines for storing a value from main memory, each of said cache lines comprised of one or more dynamic random access memory (DRAM) cells, each of said DRAM cells being refreshed each time said cache line is accessed, each of said DRAM cells reliably storing said value for a safe period; and

a timer associated with each of said plurality of cache lines, each of said timers controlling a signal that resets a valid bit associated with said cache line after said safe period.

28. The cache memory of claim 27, wherein said safe period is established based on characteristics of an integrated circuit (IC) process used to manufacture said DRAM cells.

29. The cache memory of claim 27, wherein said DRAM cells are embodied as 4-T DRAM cells.

30. The cache memory of claim 27, wherein said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N.

31. The cache memory of claim 27, wherein said timer is a k bit timer and said timer receives a tick from any source.

32. The cache memory of claim 27, wherein said timer is any k-state finite state machine (FSM) that can function logically as a counter.

33. The cache memory of claim 27, further comprising a dirty bit associated with each of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line after said decay interval.

34. A method for reducing leakage power in a cache memory, said cache memory having a plurality of cache lines, for storing a value from main memory, each of said cache lines comprised of one or more dynamic random access memory (DRAM) cells, each of said DRAM cells reliably storing said value for a safe period, said method comprising the steps of:

refreshing each of said DRAM cells each time said corresponding cache line is accessed,; and

providing a timer for each of said cache lines;

resetting said timer each time said cache line is accessed; and

resetting a valid bit associated with said cache line after said safe period.

35. The method of claim 34, wherein said safe period is established based on characteristics of an integrated circuit (IC) process used to manufacture said DRAM cells.